IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Ramachandran et al.

Serial No.: 10/696,626

Filed: October 29, 2003

Confirmation No.: 5553

Group Art Unit: 2611

Examiner: Wong, Linda

Docket No.: 03SKY0003

For: MULTI-MODE RECEIVER

REPLY BRIEF UNDER 37 C.F.R 41.41

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Sir:

This is a Reply Brief in response to the Examiner's Answer dated November 14, 2008.

I. STATUS OF THE CLAIMS

Claims 1-33 remain pending in the present application. The Examiner's Answer maintains the rejections of the claims and generally repeats the arguments advanced during prosecution of this application along with providing comments to the Appeal Brief (in the Response to Argument Section, pages 13-20 of the Examiner's Answer), the latter filed on August 20, 2008. With regard to the substantive remarks of the Examiner's Answer, Appellants disagree. Appellants will address some issues raised in the Examiner's Answer as applicable to the independent claims under appeal. Appellants continue to repeat, re-allege, and incorporate by reference the positions and arguments set forth in the Appeal Brief.

II. ARGUMENTS

A. Claims 1, 11, and 21

On pages 13-15 of the Examiner's Answer, the following is alleged (emphasis in original):

> Regarding **claims 1, 11, 21**, the appellant further contends the limitation "wherein . . . selectively DC-offset correcting comprises selecting . . . different DC-offset correcting bandwidths based on which system baseband signal is to be processed" is not disclosed by the prior art, Yan.
>
> The examiner respectfully disagrees. Yan discloses "The DC offset correction operates to force the DC levels of the differential in-phase signals I+ and I- to a common level and the DC levels of the differential quadrature signals Q+ and Q- to a common level to reduce or eliminate distortion caused by having a DC offset between the respective differential signals." (Col. 5, lines 37-42) Depending on the amount of offset found in the input baseband signal as shown in Fig. 1, labels I+, I-, Q+ and Q-, the DC correction signal would apply an amount of adjustment needed to adjust the I and Q signals to a common level. In implementation, it is implied that the DC correction circuitry will perform a selection or choice in order to determine the amount of adjustment, depending on the baseband signal inputted, needed to provide a common level as discussed in the prior art.
>
> The examiner would like to further emphasize, although the examiner uses the term "implied" in the rebuttal above, this does not indicate the prior art does not disclose the recited limitations. Yan

> discloses "adjusting the Q+, Q- and I+, I- of the DC correction signal to a common level". (Col. 5, lines 37-42) We know that in order to apply DC offset correction, Q+, Q-, I+ and I- must be at different levels. As explained above, in implementation, to adjust such components of the DC correction signal to a common level, an appropriate choice or selection of the amount of adjustment needed must be made in order to bring the I and Q signals to a common level.
>
> Furthermore, Yan discloses applying DC offset correction to baseband signals. (Fig. 1, labels I and Q are baseband signals) Such types of signals are alternating waveforms with 90 degree difference. Since DC correction is applied to such waveforms, the bandwidth or range in which the DC offset is corrected would depend on the amount of DC offset is found within the signals or waveforms.

Appellants respectfully disagree. To begin, Appellants note that I and Q are in-phase and quadrature-phase components of a single input signal having the same system baseband bandwidth. I and Q differ not in frequency but in phase. Further, I+ and I-, and Q+ and Q-, are merely differential versions of the same signal. *Yan* states the following:

> The DC offset correction operates to force the DC levels of the differential in-phase signals I+ and I- to a common level, and the DC levels of the differential quadrature signals Q+ and Q- to a common level to reduce or eliminate distortion caused by having a DC offset between the respective differential signals.
> (col. 5, lines 37-42).

Appellants respectfully submit that the quotation " 'adjusting the Q+, Q- and I+, I- of the DC correction signal to a common level' " contained in the Examiner's Answer at page 14 represents a misquoting of *Yan*, col. 5, lines 37-42. *Yan* appears to show that the I signals (I+ and I-) are adjusted to a first common level, and the Q signals (Q+ and Q-) are adjusted to a second common level. Indeed, the introduction of both levels with an "a" in the claims (*e.g.*, claim 8) further supports the fact that different levels are intended. Thus, the DC correction circuitry of *Yan*, insofar as it appears to disclose adjusting differential versions of a signal to common levels, focuses attention on the mechanisms of correcting errors introduced by downconversion rather than any mechanisms in

handling adjustments needed to address different offset correction requirements based on the selected system (e.g., CDMA, PCS, etc.).

The Examiner's Answer (page 14) alleges: "In implementation, it is implied that the DC correction circuitry will perform a selection or choice in order to determine the amount of adjustment, depending on the baseband signal inputted, needed to provide a common level as discussed in the prior art." Even assuming, *arguendo*, that the DC correction circuitry of *Yan* performs a "selection … to determine the amount of adjustment," *Yan* fails to disclose, teach, or suggest that the selection involves "selecting … different DC-offset correcting bandwidths," as recited in claim 1. The "amount of adjustment" appears to depend not on the bandwidth, but on the errors in the differential versions of the same signal (I or Q), both of which have the same bandwidth. If the circuitry of *Yan* is capable of making a different "selection or choice … to provide a common level" for two signals having the same bandwidth, clearly the particular alleged "selection or choice … to provide a common level" does not necessarily and by implication involve "selecting … different DC-offset correcting bandwidths." Even assuming, *arguendo*, the DC correction circuitry of *Yan* is provided with the components of input signals having differing system baseband bandwidths, *Yan* in no way discloses, teaches, or suggests "selecting … different DC-offset correcting bandwidths," as recited in claims 1 and 21 or "bandwidth-switchable DC-offset correction elements," as recited in claim 11. Therefore, Appellants maintain their prior traversal of this allegation and respectfully request that the rejection be overruled.

B. Claims 9 and 18

On pages 15-16 of the Examiner's Answer, the following is alleged (emphasis in original):

> Regarding claims **9, 18,** the appellant contends "the final office action (page 11) appears to allege inherency of the features of claim 9 (allegedly based on a Nyquist rate determination). ... Appellants maintain the prior traversal of this allegation, the allegation being inadequate to show why the claimed features are necessarily present in the reference, as Yan contains no discussion of different sampling rates for different signals."
>
> The examiner respectfully disagrees. The limitation under discussion recites "sampling at a first sampling rate for the first baseband signal and a second sampling rate for the second baseband signal." The examiner interpreted this limitation as the first incoming baseband signal is transmitted from one system and requires sampling at a first rate and a second incoming signal is transmitted from another system and requires sampling at a second rate. As per the final office action, Yan et al discloses a plurality of different modes or systems. (Fig. 1, labels 40a-d) The system as shown in Fig. 1 would receive plurality of signals, since the receiver continuously receives signals produced from any of the types of systems.
>
> Yan et al also discloses the baseband processor, label 30, "implemented in one or more digital signal processors", which indicates given an analog signal is inputted to the baseband processor, an analog to digital converter can be found within the digital signal processor so the DSP can operate digitally. Since I+, I-, Q+ and Q- signals are adjusted based on the mode of the received signal (Fig. 1, labels 40a-d), the signals would be sampled at a rate determined by Nyquist matching the mode of the signal. Nyquist is the basic, well known concept within the art used for determining sampling rate. By doing so, the system would not lose information needed for demodulation when transferring from analog to digital.

Appellants respectfully disagree. The Examiner's Answer alleges that "the signals would be sampled at a rate determined by Nyquist matching the mode of the signal," but that is not necessarily the case. For example, the signals of *Yan* might instead be sampled at one rate determined by Nyquist for the highest frequency of any of the signals. Thus, even assuming, *arguendo*, that the baseband processor of *Yan* digitally samples signals having differing bandwidths, one having ordinary skill in the art would recognize that it may sample at one rate and oversample some or all of the signals based on the desired performance.

Therefore, Appellants maintain their prior traversal of this inherency allegation and respectfully request that the rejection be overruled.

C. Claim 28

On page 17 of the Examiner's Answer, the following is alleged (emphasis in original):

> Regarding **claim 28**, the appellant contends the limitation "wherein ... selectively DC-offset correcting comprises selecting ... different DC-offset correcting bandwidths based on which system baseband signal is to be processed" is not disclosed by the prior art, Peterzell.
>
> The examiner respectfully disagrees. The limitation, under discussion, recites "a direct current (DC)-correction element configured to include switchable bandwidths." The examiner interprets the term "switchable bandwidths" as the bandwidth of the DC offset is switched or adjusted or changed from a current level to a new level. The limitation can also be interpreted as the range of the correction needed to eliminate DC offset is selected.

Appellants respectfully disagree with the interpretations of the Examiner. According to Appellants' specification, "[t]he MMR system adapts to the different systems by using filters and DC (direct current) offset correction elements that have switchable bandwidths." (page 3, lines 7-9). The specification also states:

> As explained below, the LP filters 214, 228 (and LP filters 220 and 232 of the AGC element 216) and DC correction elements 224 and 236 of the common baseband section 212a are adjustable (*e.g.*, have switchable bandwidths via control signals from the baseband subsystem 130, FIG. 1) to achieve the desired frequency response for the particular mode being implemented (*e.g.*, CDMA, PCS, GPS, DBS). For example, the 3-dB bandwidths for the CDMA, GPS, and DBS modes are approximately 630 kHz, 1 MHz, and 8 MHz, respectively. Further, the difference in DC bandwidth correction can be fifty-fold between various systems (*e.g.*, approximately 1 kHz for CDMA versus 50kHz for DBS), and thus the DC correction elements 224 and 236 are adjusted in a similar manner.
>
> (page 7, lines 13-23).

With all due respect, the relevant interpretation of "switchable bandwidths" is not to be based on that of the Examiner, but rather, according to well-established Federal case law,

by one having ordinary skill in the art in view of the specification. The specification clearly describes "DC (direct current) offset ***correction elements*** that have switchable bandwidths" (page 3, emphasis added) and refers to "3-dB bandwidths" expressed in signal frequencies. By contrast, a DC offset is "direct current," which inherently has zero bandwidth. Accordingly, one of ordinary skill in the art would not, in view of the specification, interpret "switchable bandwidths" as "the ***bandwidth of the DC offset*** is switched or adjusted or changed from a current level to a new level." (Examiner's Answer, page 17, emphasis added).

Further, the range of correction is not any range, but according to a selected bandwidth. Regarding *Peterzell*, the Examiner's Answer alleges:

> This indicate the amount of correction needed for DC offset correction depends on the LO drive level. In order to properly eliminate all DC offset, a selection or choice of the amount or level of adjustment is determined. Peterzell also discloses the LO drive level is varied over a range. To eliminate the DC offset cause by the LO drive level in varied range, the ***DC offset bandwidth or range must also be selected***.
> (page 19, emphasis added).

In the above allegation, the Examiner's Answer reinterprets the "DC offset bandwidth" to be "DC offset range," which contradicts the plain meaning of "bandwidth" as used in "switchable bandwidths" as recited in claim 28. Neither *Peterzell* (nor *Yan*, for similar reasons explained above and in the Appeal Brief), discloses or teaches the above-emphasized claim features, and accordingly, Appellants maintain their prior traversal of this allegation and respectfully request that the rejection be overruled.

CONCLUSION

Based upon the foregoing discussion, the Appellants respectfully request that the Examiner's final rejection of claims 1-33 be overruled and withdrawn by the Board, and that the application be allowed to issue as a patent with all pending claims.

No additional fee is believed to be due. However, any additional fee that may be due or required is authorized to be charged to deposit account no. 20-0778.

Respectfully submitted,

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